

Appln No. 10/769,488  
Amdt date August 6, 2007  
Reply to Office action of February 6, 2007

**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A logic ~~development~~ development system using an external microcomputer which replaces ~~[[for]]~~ a built-in microcomputer ~~that is~~ incorporated in an existing electronic control unit ~~for use~~, comprising:

a mother board ~~center block that includes~~ including an application facility block and a first communication facility block;

a core board ~~peripheral block that includes~~ including ~~quasi-microcomputer peripheral devices~~ one or more devices which simulate, by software, ~~[[the]]~~ peripheral devices of ~~[[a]]~~ the built-in microcomputer so as to execute an ~~input/output~~ input or output process, the core board further including a computing facility block and a second communication facility block, ~~and that is connected to said center block over a bus~~;

a peripheral component interconnect (PCI) bus coupling said mother board and said core board; and

an interface board ~~circuit block that includes~~ including circuits ~~equivalent to~~ associated with ~~[[the]]~~ hardware of said electronic control unit, wherein the interface board ~~and that is connected~~ coupled to said one or more devices via a harness ~~peripheral block~~, wherein:

said first communication facility block included in said mother board ~~center block~~ and each of said ~~quasi-microcomputer peripheral devices~~ one or more devices included in said core board ~~peripheral block~~ are ~~connected~~ coupled to each other over said PCI bus; and

said communication facility block and each of said one or more devices transfer data ~~directly~~ to or from each other over said PCI bus.

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2. (Currently Amended) A logic development system using an external microcomputer which replaces ~~[[for]]~~ a built-in microcomputer ~~that is~~ incorporated in an existing electronic control unit ~~for use~~, comprising:

a mother board ~~center block that includes~~ including an application facility block and a first communication facility block;

a core board ~~peripheral block that includes quasi microcomputer peripheral devices~~ including one or more devices which simulate, by software, ~~[[the]]~~ peripheral devices of ~~[[a]]~~ the built-in microcomputer so as to execute an ~~input/output~~ input or output process, the core board further including a computing facility block and a second communication block facility, and ~~that is connected to said center block over a bus~~; and

a peripheral component interconnect (PCI) bus coupling said mother board and said core board;

~~an interface circuit block that includes~~ interface board including circuits ~~equivalent to~~ associated with ~~[[th]]~~ hardware of said electronic control unit, wherein the interface board ~~and that is connected~~ coupled to said ~~quasi microcomputer peripheral devices~~ one or more devices via a harness peripheral block, and ~~wherein~~:

a bus controller in said computing facility block interposed between said first communication facility included block in said mother board ~~center block~~ and each of said ~~quasi microcomputer peripheral devices~~ one or more devices ~~includes a bus controller~~; wherein

said first communication facility block included in said mother board ~~center block~~ and said bus controller are ~~connected~~ coupled to each other over said PCI bus, and said bus controller and each of said ~~quasi microcomputer peripheral devices~~ one or more devices are ~~connected~~ coupled to each other over an internal bus; and

said first communication facility block and each of said ~~quasi microcomputer peripheral devices~~ one or more devices transfer data ~~directly~~ to or from each other by way of said PCI bus, bus controller, and internal bus.

3. (Currently amended) A microcomputer logic development system according to claim 1, wherein: a virtual ~~input/output register~~ memory device is interposed between said communication block included in said ~~center block~~ mother board and said PCI bus; and when transfer data is temporarily recorded in said virtual ~~input/output register~~ memory device at the timing of receiving or transmitting data, said virtual ~~input/output register~~ memory device behaves like ~~an input/output register~~ a memory device included in ~~an actual~~ the built-in microcomputer.

4. (Currently amended) A microcomputer logic development system according to claim 1, wherein: an object on which said application ~~facility~~ block acts is a vehicle; said logic development system includes an ignition switch; and when said logic development system is interlocked with ~~[[the]]~~ an on or off state of said ignition switch, control software for said vehicle is initiated or terminated in the same manner as ~~the one~~ control software residing in said ~~actual~~ electronic control unit.

5. (Currently amended) A microcomputer logic development system according to claim 4, wherein~~[[:]]~~ said circuits that are included in said ~~interface circuit block~~ interface board and ~~equivalent to~~ associated with the hardware of said electronic control unit include at least ~~[[on]]~~ one facility circuit in which a microcomputer is incorporated; and said facility circuit is not actuated with the on state of said ignition switch but is actuated synchronously with ~~the timing of starting up of the center block~~ the timing of starting up of the mother board.

6. (Currently amended) A microcomputer logic development system according to claim 5, wherein said facility circuit includes a power circuit that is actuated with the on state of said ignition switch, and a logic circuit which actuates the microcomputer in the facility circuit ~~[[that]]~~ when both a signal sent from said power circuit and a signal sent from said ~~center block~~ mother board become valid, ~~actuates said microcomputer~~.

7. (Currently amended) A microcomputer logic development system according to claim 4, wherein: when said ignition switch is turned off, data that should be held is stored in

either of a memory included in an external storage device ~~connected~~ coupled to said logic development system ~~[[and]]~~ or a memory included in said logic development system; when said ignition switch is turned on, data that should be held is read from said external storage device and restored; and the same capability as the capability of a backup memory is thus realized for said logic development system.

8. (Currently amended) A microcomputer logic development system according to claim 4, wherein initial values to ports are set ~~are determined~~ within an initialization routine which is executed on said ~~center-block~~ mother board ~~[[until]]~~ when said ignition switch is turned on after the power supply of said logic development system is turned on.

9. (Currently amended) A microcomputer logic development system according to claim 1, wherein: said PCI bus contains a one-channel interrupt signal line over which an interrupt request is issued from said ~~peripheral-block~~ core board to said ~~center-block~~ mother board; when said interrupt signal line is activated by said ~~peripheral-block~~ core board, said application block included in said ~~center-block~~ mother board accepts an interrupt request; and after the interrupt request is accepted, said interrupt signal line is inactivated.

10. (Currently amended) A microcomputer logic development system according to claim 9, wherein when interrupt handling is terminated, said application block included in said ~~center-block~~ mother board checks if said interrupt signal line is inactive.

11. (Currently amended) A microcomputer logic development system according to claim 10, wherein when interrupt handling is terminated, if said interrupt signal line is active, said application block included in said ~~center-block~~ mother board inactivates said interrupt signal line.

12. (Currently amended) A microcomputer logic development system according to claim 1, wherein: said computing block included in said ~~peripheral-block~~ core board includes a facility for temporarily fetching data; when a large amount of data is transferred between said

~~center-block~~ mother board and each of said ~~quasi-microcomputer peripheral devices~~ one or more devices included in said ~~peripheral-block~~ core board, the large amount of data is transferred in a burst mode between said ~~center-block~~ mother board and said computing block, and transferred in a non-burst mode between said computing block and each of said ~~quasi-microcomputer peripheral devices~~ one or more devices.

13. (Currently amended) A microcomputer logic development system according to claim 9, wherein after said application block included in said ~~center-block~~ mother board accepts an interrupt request, said application block acquires interrupt flags from each of said ~~quasi-microcomputer peripheral devices~~ one or more devices over said PCI bus; after said application block acquires interrupt flags, said application block clears the interrupt flags present in each of said ~~quasi-microcomputer peripheral devices~~ one or more devices.

14. (Currently amended) A microcomputer logic development system according to claim 13, wherein after said application block included in said ~~center-block~~ mother board acquires interrupt flags, said application block executes a process associated with each of the acquired interrupt flags.

15. (Currently amended) A microcomputer logic development system according to claim 9, wherein: after said application block included in said ~~center-block~~ mother board accepts an interrupt request, said application ~~facility~~ block acquires a plurality of interrupt flags from each of said ~~quasi-microcomputer peripheral devices~~ one or more devices over said PCI bus; said application ~~facility~~ block selects one interrupt flag assigned a high priority, and executes a process associated with the interrupt flag; and after the process is completed, said application ~~facility~~ block clears a process completion interrupt flag present in each of said ~~quasi-microcomputer peripheral devices~~ one or more devices.

16. (Currently amended) A microcomputer logic development system according to claim 15, wherein after said application block selects one interrupt flag assigned a high priority, and executes a process associated with the interrupt flag, said application block re-acquires a

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plurality of interrupt flags from each of said ~~quasi-microcomputer peripheral devices~~ one or more devices over said bus.

17. (Currently amended) A microcomputer logic development system according to claim 13, wherein said interrupt flags are concurrently stored at successive addresses in one of one or more registers included in each of said ~~quasi-microcomputer peripheral devices~~ one or more devices.

18. (Currently amended) A microcomputer logic development system according to claim 17, wherein: a plurality of ~~peripheral blocks~~ core boards are included; interrupt flags representing interrupts caused by each of a plurality of resources that are included in each of said ~~peripheral blocks~~ core boards are stored in a register included in each of said ~~peripheral blocks~~ core boards; the interrupt flags representing interrupts caused by each of the resources included in the first ~~peripheral block~~ core board are stored in the register included in the first ~~peripheral block~~ core board; and an extension interrupt flag indicating whether interrupt flags, representing interrupts caused by each of the resources included in each of the remaining ~~peripheral blocks~~ core boards, are present is stored in association with ~~ach peripheral block~~ each core board.

19. (Currently amended) A microcomputer logic ~~dev-lopment~~ development ~~[[syst m]]~~ system according to claim 18, ~~wh-rein~~ wherein if said extension ~~int-rupt~~ interrupt flag demonstrates that interrupt flags are stored in the register included in any of the remaining ~~peripheral blocks~~ core boards, said application block acquires the interrupt flags from the register in the remaining ~~peripheral block~~ core board.

20. (Currently amended) A microcomputer logic development system according to claim 1, wherein: a plurality of ~~peripheral blocks~~ core boards are included; the first ~~peripheral block~~ core board alone includes a free-run timer; said first ~~peripheral block~~ core board includes at least resources that act synchronously with the timer value of said free-run timer; and the remaining ~~peripheral block~~ core boards include resources independent of said free-run timer.

21. (Original) A microcomputer logic development system according to claim 20, wherein: the resources that act synchronously with the timer value of said free-run timer include a comparator and a capture unit; and the resources independent of said free-run timer include a pulse-width modulator (PWM), a communication unit, an A/D converter, and ports.

22. (Currently Amended) A logic development system using an external microcomputer which replaces ~~[[for]]~~ a built-in microcomputer ~~that is~~ incorporated in an existing electronic control unit ~~for use~~, comprising:

a mother board ~~center block that includes~~ including an application facility block;

a core board ~~peripheral block that includes~~ quasi-peripheral including one or more devices which simulate, by software, ~~[[the]]~~ peripheral devices of ~~[[a]]~~ the built-in microcomputer so as to execute an input/output input or output process; and

a peripheral component interconnect (PCI) bus over which said mother board ~~center~~ ~~block~~ and said core board ~~peripheral block~~ are ~~connected~~ coupled to each other, wherein:

when an interrupt factor occurs in any of said ~~quasi-peripheral device~~ one or more devices, said application facility block reads or writes data in or from said ~~quasi-peripheral device~~ one or more devices; and

data whose ~~pre-ssing~~ processing speed is requested to be low is read or written all ~~together~~ together during communication performed before or after ~~[[the]]~~ action of said application facility block.

23. (Currently Amended) A logic development method for a microcomputer requiring including a mother board ~~center block that includes~~ having an application facility block, a core board ~~peripheral block that includes~~ quasi-microcomputer peripheral devices having one or more devices which simulate, by software, ~~[[the]]~~ peripheral devices of ~~[[a]]~~ the built-in microcomputer so as to execute an input/output input or output process, an interface board ~~circuit block that includes~~ having circuits ~~equivalent to~~ associated with ~~[[the]]~~ hardware of

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an electronic control unit, and a peripheral component interconnect (PCI) bus over which said mother board ~~center block~~ and said core board ~~peripheral block~~ are ~~connected~~ coupled to each other, said microcomputer logic development method comprising ~~the steps of:~~

issuing an interrupt request from said core board ~~peripheral block~~ to said mother board ~~center block~~ over a one-channel interrupt signal line contained in said PCI bus;

accepting the interrupt request when said interrupt signal line is activated ~~by means of~~ via said ~~peripheral block~~ core board; and

inactivating said interrupt signal line after the interrupt request is accepted.

24. (Currently amended) A microcomputer logic development method according to claim 23, further comprising the steps of:

after an interrupt request is accepted, acquiring interrupt flags from each of said ~~quasi microcomputer peripheral devices~~ one or more devices over said bus; and

after the interrupt flags are acquired, clearing the interrupt flags from each of said ~~quasi microcomputer peripheral devices~~ one or more devices.

25. (New) The microcomputer logic development system of claim 2, wherein the computing block is a microcomputer, and the bus controller in the microcomputer is configured to control flow of information between the mother board and the one or more devices.